

Claims

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A thin film transistor comprising:

a gate electrode disposed on a predetermined substrate and formed in a predetermined pattern;

a semiconductor layer formed correspondingly to patterning of said gate electrode;

a pixel electrode interposed by said semiconductor layer; and

a signal electrode interposed by said semiconductor layer and disposed at a predetermined interval from said pixel electrode,

wherein said signal electrode is disposed at such a position where said signal electrode prevents crosstalk running from an adjacent signal electrode, via said semiconductor layer, to said pixel electrode.

2. The thin film transistor according to Claim 1, wherein said semiconductor layer is formed in an almost equivalent pattern to said patterning of said gate electrode.

3. The thin film transistor according to Claim 1, wherein:

1 said gate electrode is provided on said
2 substrate; and

3
4 said semiconductor layer is formed on said gate
5 electrode through a gate insulating film and pattern-
6 formed correspondingly to said patterning of said gate
7 electrode.

1 4. The thin film transistor according to Claim 1,
2 wherein said semiconductor layer is formed on a layer
3 lower than a gate insulating film formed on said lower
4 layer of said gate electrode.

5
6 5. A thin film transistor comprising:

7
8 a source electrode provided on a predetermined
9 insulating substrate;

10
11 a drain electrode disposed by keeping a
12 predetermined interval from said source electrode;

13
14 a semiconductor layer disposed so as to contact
15 said source electrode and said drain electrode and
16 connect said both electrodes each other;

17
18 a gate insulating film for covering said
19 semiconductor layer; and

20
21 a gate electrode disposed adjacently to said
22 gate insulating film; wherein said gate electrode is
23 patterned by being provided with a protruded portion
24 almost orthogonal to said source electrode and said drain

25 electrode and said semiconductor layer and said gate
26 insulating film are pattern-formed in accordance with
27 said patterning of said gate electrode, and
28

29 said drain electrode is disposed nearby said
30 root of said protruded portion on said gate electrode to
31 said source electrode.

1 6. The thin film transistor according to Claim 5,
2 wherein said semiconductor layer and said gate insulating
3 film are formed in said same patterning process as said
4 gate electrode.

1 7. The thin film transistor according to Claim 5,
2 wherein said source electrode and said drain electrode
3 are arranged in parallel with each other at a
4 predetermined line width.

1 8. A liquid-crystal display panel having a pixel
2 electrode and a thin-film-transistor-channel structure
3 for applying a voltage to said pixel electrode,
4 comprising:
5

6 a gate line for forming a gate electrode in
7 said thin-film-transistor-channel structure; and
8

9 a signal line connected to a signal electrode
10 in said thin-film-transistor-channel structure; and
11

12 a semiconductor layer to be patterned under a
13 state along said gate line by exceeding said thin-film-
14 transistor-channel structure; wherein

15 said signal electrode is configured so as to
16 prevent said current incoming through said semiconductor
17 layer from an adjacent signal line for applying a voltage
18 to a pixel electrode adjacent to said former pixel
19 electrode.

1 9. The liquid-crystal display panel according to Claim
2 8, wherein said semiconductor layer remains on said gate
3 line and has a parasitic thin film transistor between
4 said adjacent signal line and said thin-film-transistor-
5 channel structure.

1 10. The liquid-crystal display panel according to Claim
2 8, wherein said gate electrode is formed on a substrate
3 and said semiconductor layer is formed on a layer upper
4 than said gate insulating film formed on said upper layer
5 of said gate electrode.

1 11. The liquid-crystal display panel according to Claim
2 8, wherein said semiconductor layer is formed on a layer
3 lower than said gate insulating film formed on said lower
4 layer of said gate electrode.

1 12. A thin film-transistor manufacturing method
2 comprising:

3
4 an opaque film step of forming an opaque film
5 having a predetermined shape on a substrate:

6
7 an insulating film step of forming an
8 insulating film on said substrate so as to cover said
9 opaque film;

10 a source-and-drain-electrode forming step of
11 forming a source electrode and a drain electrode which
12 are made of metallic films having a predetermined line
13 width and keeping a predetermined interval from each
14 other on said formed insulating film;

15
16 a semiconductor-insulating-film-layer step of
17 forming a semiconductor layer and a gate insulating film
18 layer on said insulating film in order above said source
19 electrode and said drain electrode;

20
21 a gate-electrode forming step of forming a
22 metallic film for a gate electrode on said gate
23 insulating film layer;

24
25 a pattern forming step of patterning said
26 semiconductor layer, said gate insulating film layer, and
27 said metallic film for a gate electrode and forming a
28 protruded TFT portion having a thin-film-transistor-
29 channel structure and in which said semiconductor layer
30 and said gate insulating film layer are formed at said
31 position of said gate electrode exceeding said protruded
32 TFT portion; wherein

33
34 said source-and-drain-electrode forming step
35 forms at least either of a source electrode and a drain
36 electrode serving as a signal electrode so as to cross
37 said protruded TFT portion formed in said pattern forming
38 step.

1 13. The thin-film-transistor manufacturing method
2 according to Claim 12, wherein said pattern forming step

1 pattern-forms said semiconductor layer, said gate
2 insulating film layer, and said metallic film for a gate
3 electrode in said same patterning step.

1 14. The thin-film-transistor manufacturing method
2 according to Claim 12, wherein said pattern forming step
3 pattern-forms said semiconductor layer, said gate
4 insulting film layer, and said metallic film for a gate
5 electrode into almost said same shape.